SILICON DEVICE PERFORMANCE MEASUREMENTS
TO SUPPORT TEMPERATURE RANGE ENHANCEMENT

Cooperative Agreement NCC3-175

NASA
Lewis Research Center
Cleveland, Ohio

Semi-Annual Report
May 7, 1991 - November 9, 1991

Prepared by:

James Bromstead
Bennett Weir
R. Wayne Johnson, Principal Investigator
Ray Askew, Principal Investigator

December 2, 1991

Auburn University
Center for the Commercial
Development of Space Power
231 Leach Center
Auburn, AL 36849

INTRODUCTION

This report details the efforts made since the last report was issued. The results of the NPN bipolar transistor (BJT) (2N6023) breakdown voltage measurements have been analyzed. Switching measurement have been made on the NPN BJT, the insulated gate bipolar transistor (IGBT) (TA9796) and the N-channel metal-oxide-semiconductor field effect transistor (MOSFET) (RFH75N05E). Efforts have also been made to build an H-bridge inverter. Also discussed in this report are the plans that have been made to do life-testing on the devices, to build an inductive switching test circuit and to build a dc/dc switched mode converter.

BJT BREAKDOWN VOLTAGE

Figure 1. shows the results from the BJT breakdown measurements. Breakdown voltage in a power device is determined to a first order by the doping concentration in the epitaxial layer and increases in the mean free path. This relation is demonstrated by the equation below. The figure shows an expected initial increase in breakdown voltage with temperature (about 5% per 100°C), with a sudden decrease in breakdown voltage after 150°C.

$$V_{br} = \frac{\varepsilon}{2q} \frac{E_{br}^2}{N_{epi}}$$

Where ε is the permittivity of Si, E_{br} is the critical breakdown field for the doped Si and N_{epi} is the doping concentation.

This curve was typical of several BJTs (2N6032) tested. Analysis of this phenomenon concluded increases in both the internal base resistance and base-emitter leakage currents were creating an internal base emitter voltage which begins to turn the device on. The breakdown voltage at 200°C is approximately 10% below the value at 25°C and should not significantly restrict designs at 200°C.

SWITCHING MEASUREMENTS

The major area of work since the last report has been switching tests on the N-MOSFET, BJT and IGBT. Problems in drive circuitry and resistive power loads have greatly delayed these tests.

As with the previous tests, only the heat sink mounted device was placed in the test chamber. This configuration introduced large lead inductances. Even with twisted pairs for the gate/base drive and supply/load leads, ringing persisted in the output due to lead inductances. A major concern was the reduction of these inductances to minimize the ringing.

The evolution of the switching test drive circuit is shown in Figure 2. The first circuit was fabricated as a chip and wire hybrid and placed with the device in the test chamber to reduce the drive lead inductances. This drive circuit was later abandoned due to insufficient current from the totem pole output to drive the MOSFET and IGBT. The next drive circuit tested uses the IR2110 High Voltage MOSFET gate driver. This circuit proved the fastest means of switching the N-MOSFET. The third circuit, although slower, provided the higher current drive needed for the BJT and proved adequate for the IGBT.

Problems persisted in the construction of a purely resistive load. In its final form the load consisted of a parallel combination of 10 Ω, 7 W composite power resistors which were placed in the test chamber with the device. This produced loads with a low temperature coefficient of resistance (TCR), but sizable inductances (R_L=0.67Ω L_L=0.121μH and R_L=5.56 Ω L_L=1.21μH as measured by an HP 4275A Multi-frequency LCR Meter at 10MHz).

Testing was performed by mounting the device and load in a Delta Design 9023 test chamber. Twisted pair leads (<8 inch long) connected the device to the gate/base drive circuit (driven by the Tektronics AFG5101 Arbitrary Function Generator) and the load to the voltage supply (HP6032 Power supply). Output waveforms were captured using a Tektronics 2440 oscilloscope, AM503 current amp with A6303 current probe and Tektronics HC1000 color plotter, Figure 2A. Between each test the heat sink and device were allowed to settle to the ambient chamber temperature. Tests were preformed using 100μsec pulses and a duty cycle of 1 second to avoid junction heating

Figures 3-6 show typical N-MOSFET turn-off and turn-on waveforms at 20°C and 200°C, for a $V_{DS} = 30V$, $I_D = 45A$ (Channel 1 - drain-source voltage @5V/Div, Channel 2 - drain current @10A/Div). Ringing in the turn-off voltage, Figures 3 and 5, waveforms was a result of natural oscillation between the R, L of the load and the C_{gd} of the FET. A 25 Ω gate resistor reduced the ringing in the output, but increased rise and fall times. The graph of switching time versus temperature, Figure 7, shows an almost flat response to temperature, but with switching time much higher than specified by the manufacturer. The 0.67Ω load used in the test has a time constant, $t_{RL} = 316ns$, which results in a 10-90% time of 694ns. This value contributed heavily to our room temperature I_D fall time of 620ns which is an order of magnitude longer than the manufacturer's specified typical fall time of 17ns.

In addition to the RL time constant of the load, drive limitations of the IR2110 and the charge-transfer characteristics of the RFH75N05E also contribute to the slow switching times. As in most FETs the input impedance of a power MOSFET consists of a high input resistance in parallel with an equivalent input capacitance, consisting of the gate to source, C_{gs}, and the gate to drain capacitance, C_{gd}. Due to the Miller effect on C_{gd}, the input capacitance of the MOSFET is not well-defined. The effects of the change in the input capacitance can be seen in the charge transfer characteristic of the RFH75N05E MOSFET, Figure 8 [Harris Semiconductor RFH75N05E data sheet], the normalized V_{GS} voltages and corresponding V_{DS} voltages for the FET.

Each of the V_{GS} curves can be viewed as three separate regions of turn-on or turn-off operation. In the first region of turn-on, the V_{GS} curve is linear, the gate voltage has risen to a level where there is drain current conduction. During this period, the gate potential is in the pre-threshold region, and charging the equivalent input capacitance, C_{gd}, thus the slope is fairly constant. The rate of charging in this first region directly affects the turn-on delay. In the second region, turn-on is complete when the drain voltage has switched 90%. There is an abrupt increase in the input capacitance, identified by the flattening of the gate-voltage curve. As the MOSFET turns on, the Miller effect becomes more dominant. C_{gd}, and C_{gs} being depletion-dependant are thus voltage-dependant and change rapidly in this region. In the third region, since C_{gd} is depletion dependant, its capacitance rises dramatically as the voltage between drain and gate

diminishes, and changes polarity when V_{DS} drops below V_{GS}. As C_{gd} rises, the Miller capacitance increases even more rapidly, despite the decrease in voltage gain (dV_{DS}/dV_{GS}). The increasing Miller capacitance keeps the gate-voltage characteristic nearly flat until V_{SAT} is reached. After the V_{DS} voltage has decayed to V_{SAT}, the gate then resumes its rise to the imposed gate drive level.

Figures 9-12 show typical BJT turn-off and turn on waveforms, for a $V_{CE} = 30V$ and $I_C = 45A$. Again ringing in the turn-off voltage, Figures 9 and 11, is due to the inductive load. The maximum specified rise time for the 2N6032 is 1µs and the maximum specified fall time is also 1µs. The values measured at 20°C, V_{CE} rise time of 180ns and a V_{CE} fall time of 120ns, fall well within the maximums specified by the manufacturer. A graph of the change in switching times for the BJT, Figure 13, indicates a fairly flat response in the turn-off voltage and the turn-on current. Most notable in the figure is a 5.59 ns/°C increase in the BJT turn-off current and turn on voltage times. This rate of increase is noted in the turn-off current after 150°C.

Figures 14-17 show the IGBT turn-off and turn-on waveforms at 20°C and 200°C, for a $V_{DS} = 150V$, $I_C = 30A$. Ringing in the turn-off voltage waveforms is again a result of the inductive load. A rise time of 250ns and a fall time of 1.214µs were measured for V_{CE} at 20°C. The measured fall time is less than the specified typical value of 1.8µs. The time constant for the 5.56Ω load used is 0.218µs which results in a 10-90% time of 0.479µs. This indicates that the load and temperature do not contribute to the measured times, as shown in Figure 18.

Figures 7, 13 and 18 show a graphical representation of the rise and fall times for the devices. These graphs show a fairly flat response of switching time over the 20°C to 200°C operating temperature. Because the rise and fall times were relatively unaffected by temperature in this switching test it can be seen that all the devices tested still switched at useful speeds even at 200°C.

H-BRIDGE CONVERTER

As part of the lifetime testing, an H-Bridge converter has been designed and built, Figures 19 and 20. With an operating frequency of ~21.5kHz and parallel resonant load, the inverter offered a design in which both the N-MOSFET and IGBT could be used as the switching elements. A problem encountered in the testing the MOSFET version of the inverter has been feedback between the H-Bridge and the gate driver circuitry.

"Hard" driving of the high-side transistors caused coupling of the high voltage power supply with the driver power supply through the same "Miller effect" capacitance found in the MOSFET switching tests. This coupling resulted in ringing on the +15V line. The ringing in the +15V supply line created changes in the UC3860's V_{REF} and I_{VFO} , resulting in changes in the frequency and width of the UC3860's alternating drive pulses. This led to failures in the IR2110 high-side drivers. Increasing the bypass capacitance on the +15V line did not help with the oscillation. As a solution to this problem the voltage supplies of the UC3860 and IR2110s have been separated. Reducing the IR2110 supply to +14V has also helped to reduce ringing in the gate drive.

Figures 21-24 show operating waveforms of the MOSFET inverter at 20°C. Figures 21 and 22 show the drain-source voltage ,V_{DS} , (Channel 1-20V/Div) and gate-source voltage ,V_{GS} , (Channel 2 -10V/Div) of M3, a low-side device, and M4, a high-side device, respectively. Due to the limitation in rated drain-source voltage of the RFH75N05E to 50V, (M4 ~45V), the peak V_{DS} limited the operation of the inverter to a peak device drain current ,I_D, of 5.8A. Reduction in the load resistance will allow operation at increased current by reducing the load voltage. The V_{DS} and I_D, of the low-side device M3 are shown in Figure 23, (Channel 1- 20V/Div, Channel 2- 2A/Div), note the commutation of current through the MOSFETs body diode. In our configuration, the natural frequency of the RLC load can be seen to be higher than the inverter switching frequency, thus the diode current should be commutated by the companion FET in the totem pole. But due to the split inductor configuration, the diode current is commutated in the opposing part of the totem pole, and diode recovery problems at higher current will occur. Detail of the forward conduction of the body diode is shown in Figure 24. To remedy the commutation problem the circuit is being reconfigured with a

Schottky diode (MBR3535) added in series with each FET and a fast recovery diode (1N3891) in parallel with each FET/Schottky combination as the free-wheeling diode. Reverse current now will then flow through the fast recovery diode, and because of the fast reverse recovery nature of the diode, the current during recovery will be reduced. In the IGBT version of the inverter, the free-wheeling diode is also necessary.

FUTURE PLANS

Life-Testing

Life-testing will be accomplished by running the devices in the configuration detailed in the section on the H-bridge inverter. An inductive switching test will also be performed on the devices. A test circuit will be designed.

Failure Analysis

Failure analysis has begun with N-MOSFET that failed under testing, Figure 25. This device no longer responsed to gate drive and produces a resistive I-V characteristic on the curve tracer. It is thought that the source metalization has "punched through" to the drain. After the passivation layer of SiO_2 and source aluminum have been etched and the source-channel will be Argon sputter-etched in an Auger system to profile the elemental content of the junction.

DC/DC Switch Mode Converter

Plans have been made to design a dc/dc switched mode converter. Figure 26. shows the flyback converter configuration which has been selected as the basic converter topology. The design will be implemented using IGBT's and will convert 18V to 120V at a power level of 100W.

Thick film hybrid technology will be used to construct the control circuitry. The materials used in thick films are processed in excess of 800°C and are very stable at 200°C. LM555's are currently being considered for use in the control circuit and will soon be characterized at elevated temperatures.
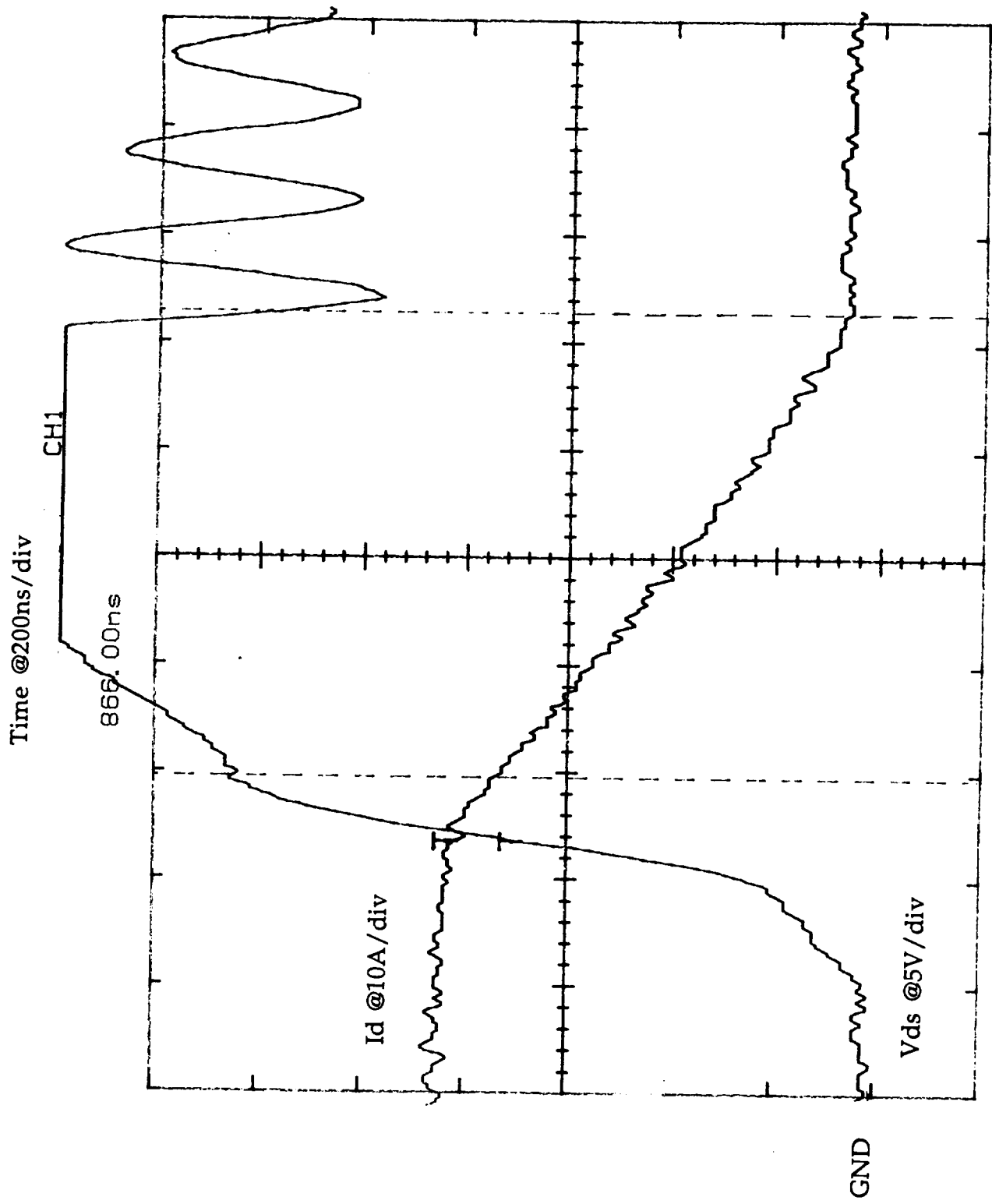
Breakdown Voltage Versus Temperature
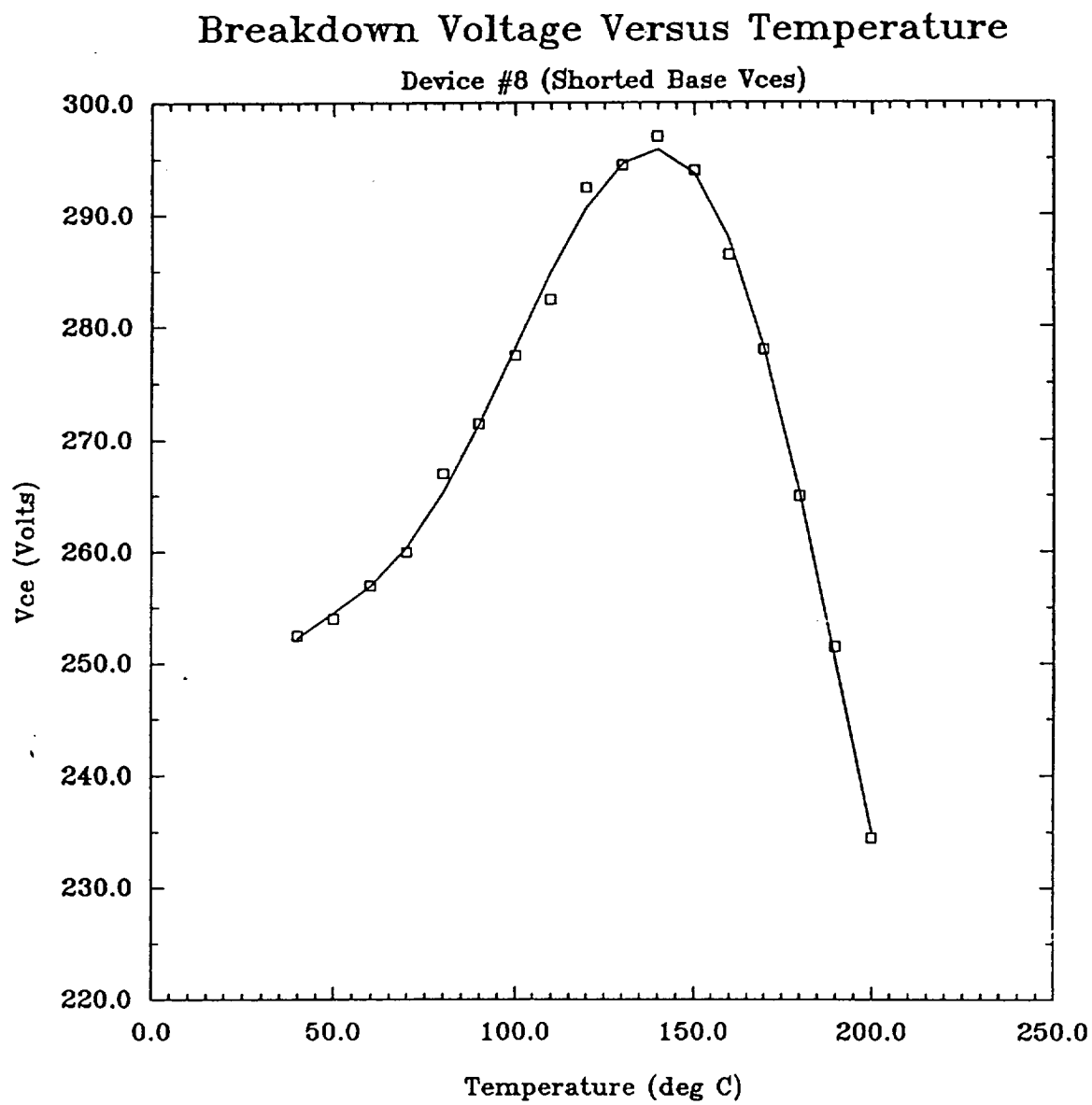
Figure 1. BJT breakdown voltage.
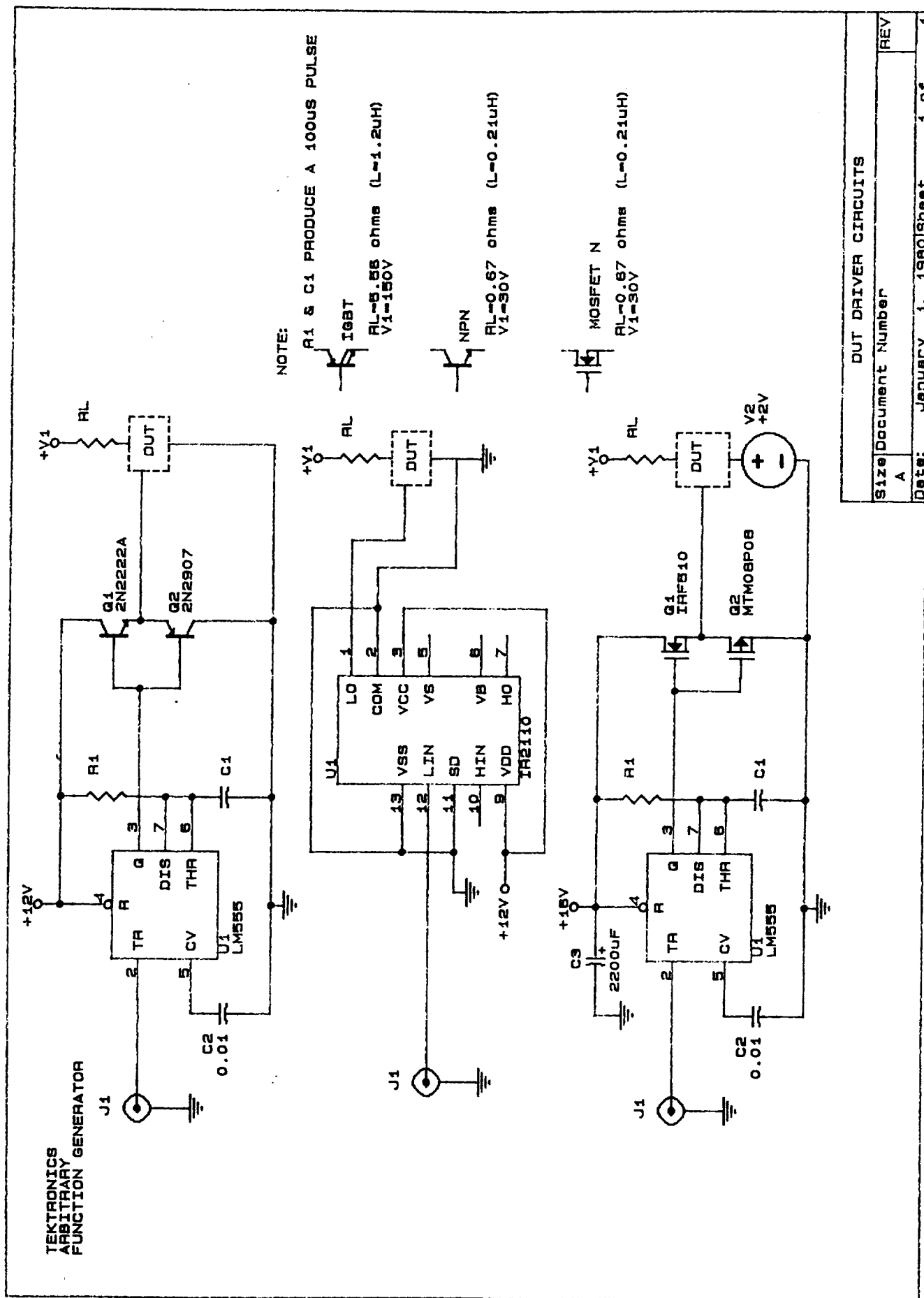
Figure 2. Driver circuits.

Figure 3. RFH75N05E MOSFET turn off at 20°C (866ns 90-10% Id fall-time).

Time @500ns/div   CH1

1.7650μs

Vds @5V/div

Id @10A/div

GND
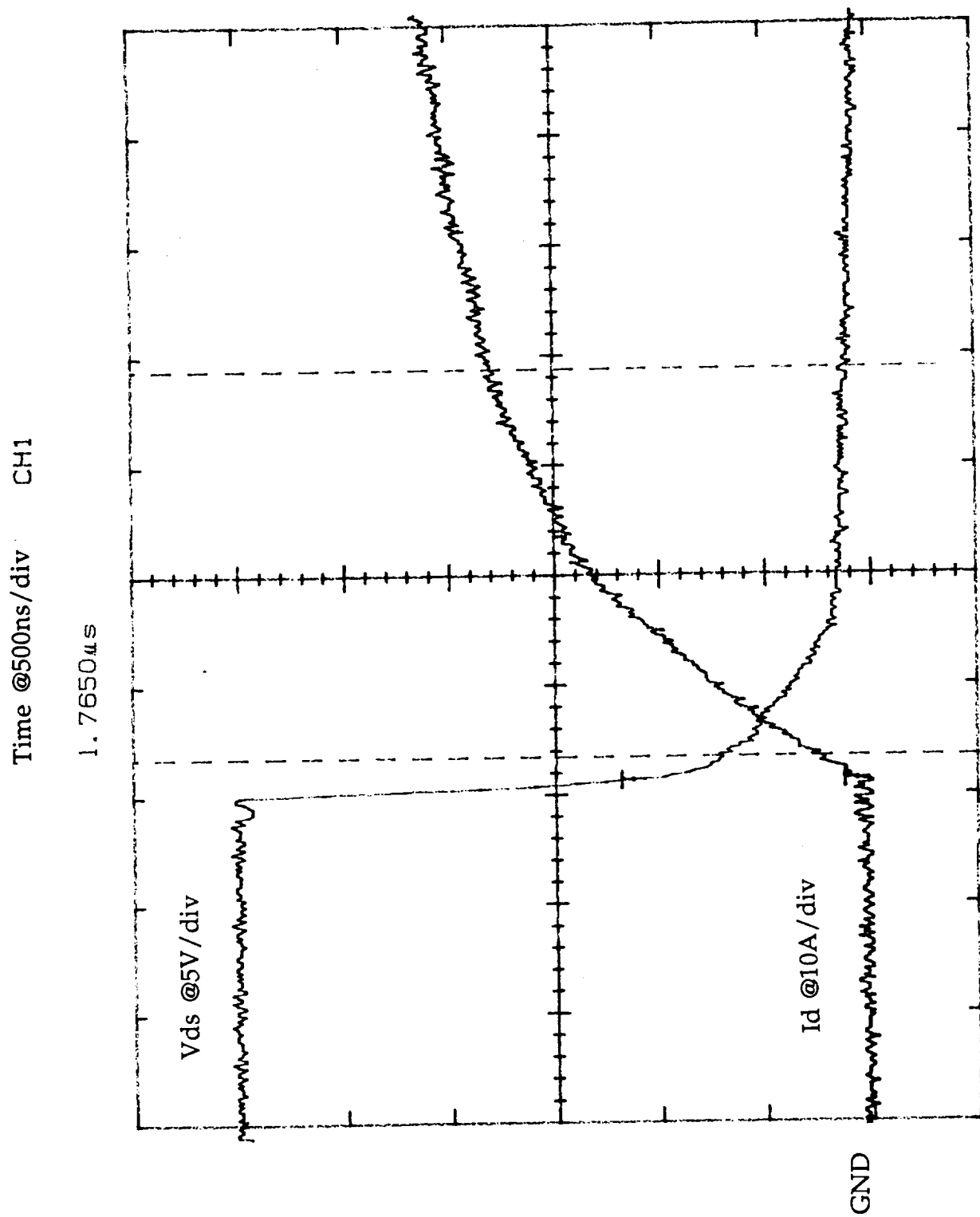
Figure 4. RFH75N05E MOSFET turn on at 20°C (1.765μs 10-90% Id rise-time).
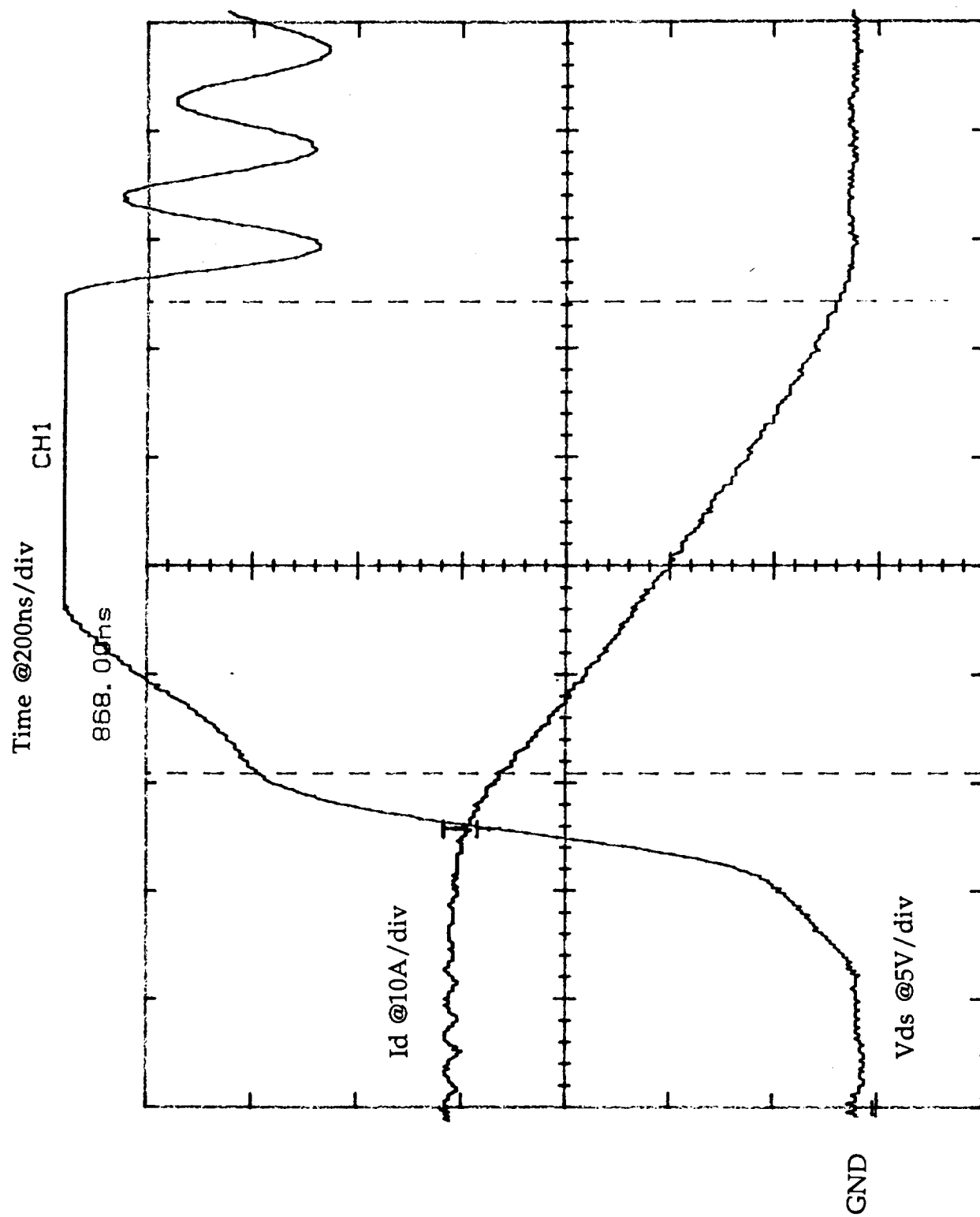
Figure 5. RFH75N05E MOSFET turn off at 200°C (868ns 90-10% Id fall-time).
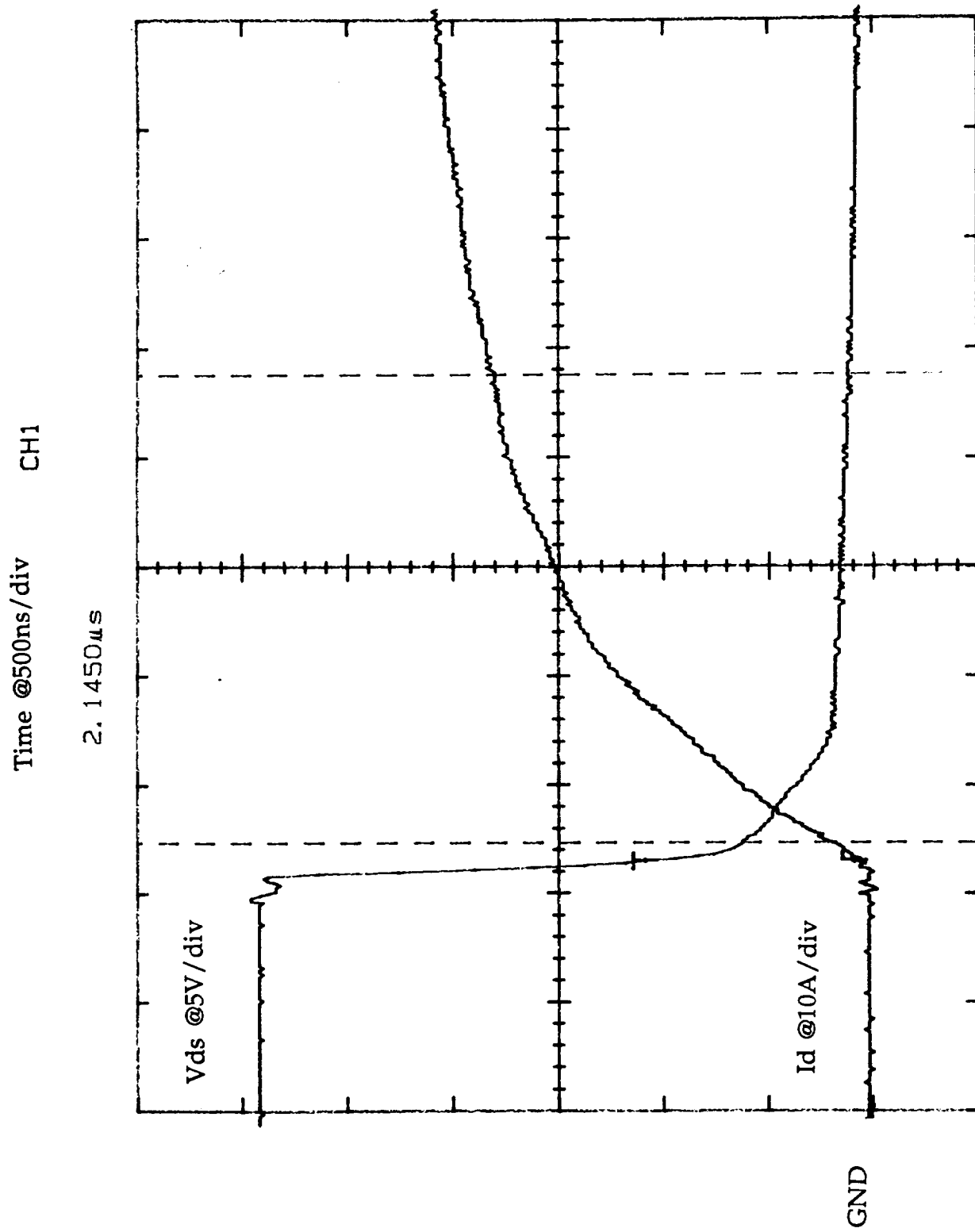
Time @500ns/div   CH1

2.1450µs

Vds @5V/div

Id @10A/div

GND

Figure 6. RFH75N05E MOSFET turn off at 200°C (2.145µs 10-90% Id rise-time).
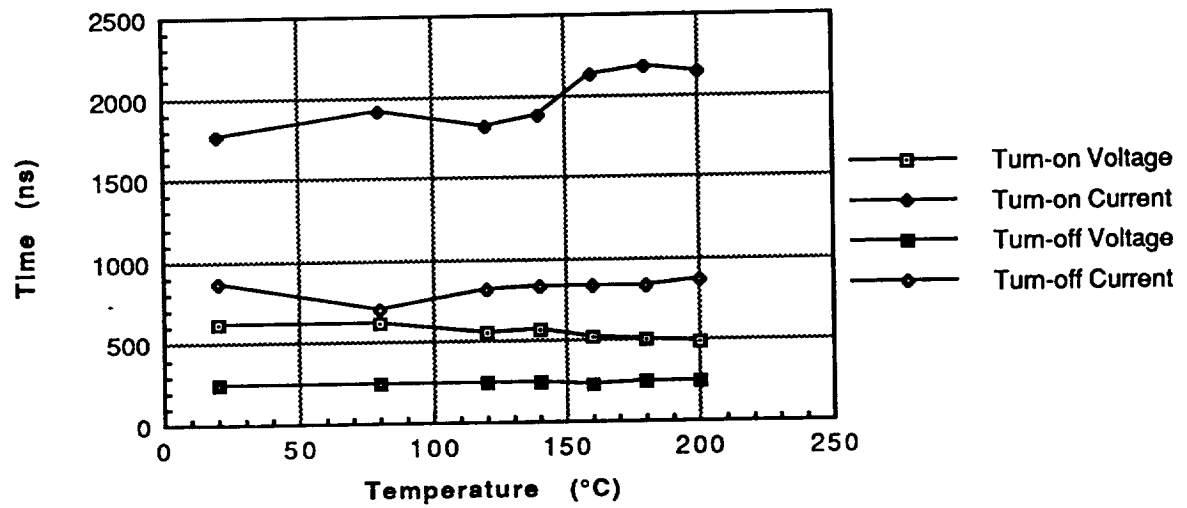
Figure 7. Resistive switching times for NMOS (RL=0.67Ω L=0.212μH).

NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT
GATE—CURRENT

V_{gs}—VOLTS

10

5

0

SWT75N05

$RL=0.867$ OHMS
$Ig(REF)=3.0$ mA
$V_{gs}=10V$

Vdd=Vdss

0.75Vdss
0.50Vdss
0.25Vdss

GATE
SOURCE
VOLTAGE

80 $\dfrac{Ig(REF)}{Ig(ACT)}$

DRAIN—SOURCE VOLTAGE

TIME—MICROSECONDS

0.75Vdss
0.50Vdss
0.25Vdss

region 3

region 2

region 1

20 $\dfrac{Ig(REF)}{Ig(ACT)}$

50

37.5

25

12.5

0

V_{ds}—VOLTS
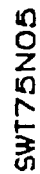
Figure 8. MOSFET charge transfer characteristics.

Time @1μs/div

CH1

Vce @10V/div

Ic @10A/div

CH1gnd

CH2gnd
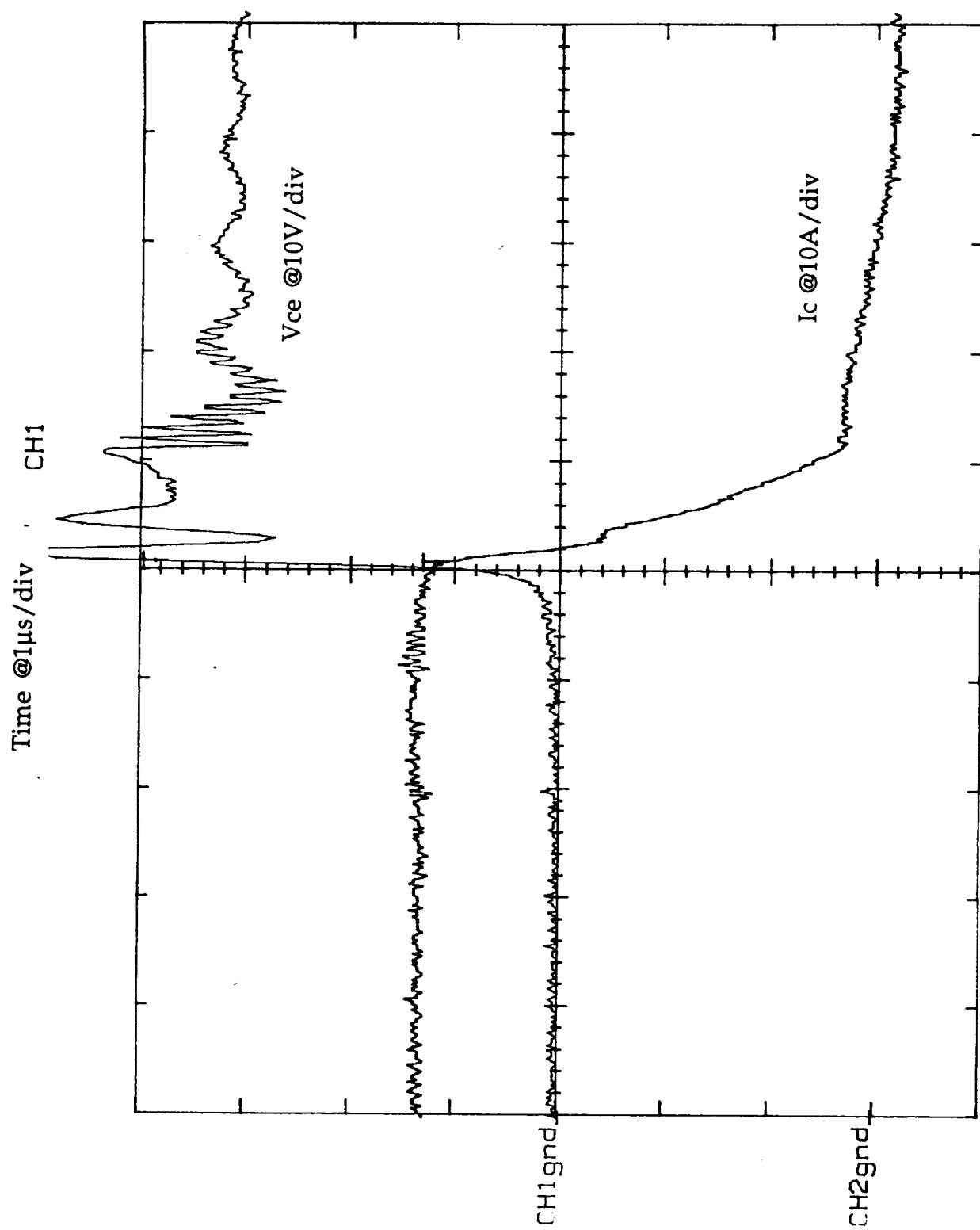
Figure 9. 2N6032 BJT turn off at 20°C.

Vce @10V/div

CH1gnd

Ic @10A/div

CH2gnd
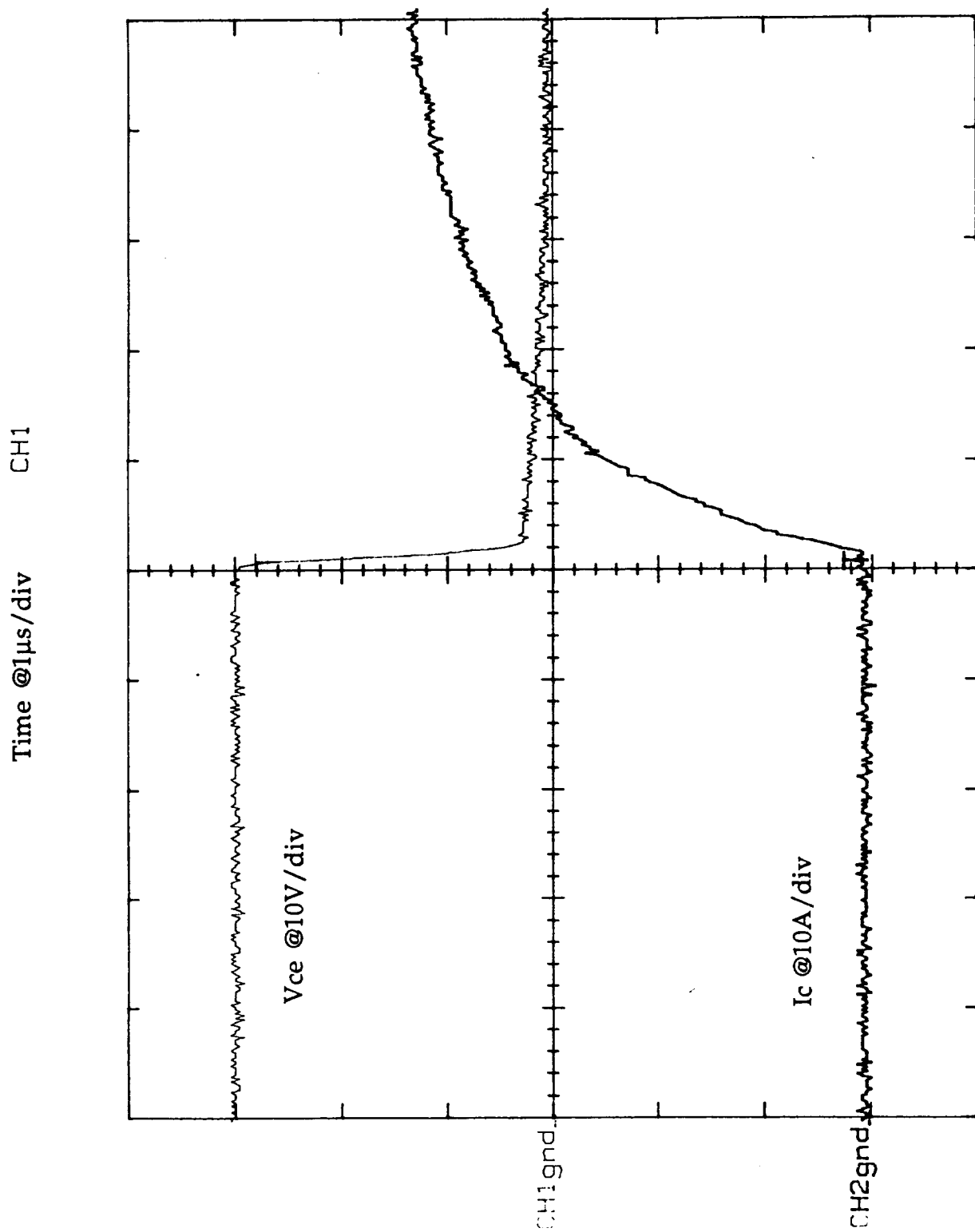
Figure 10. 2N6032 BJT turn on at 20°C.

Time @1μs/div   CH1

1.4700μs

Vce @10V/div

Ic @10A/div

CH1gnd

CH2gnd
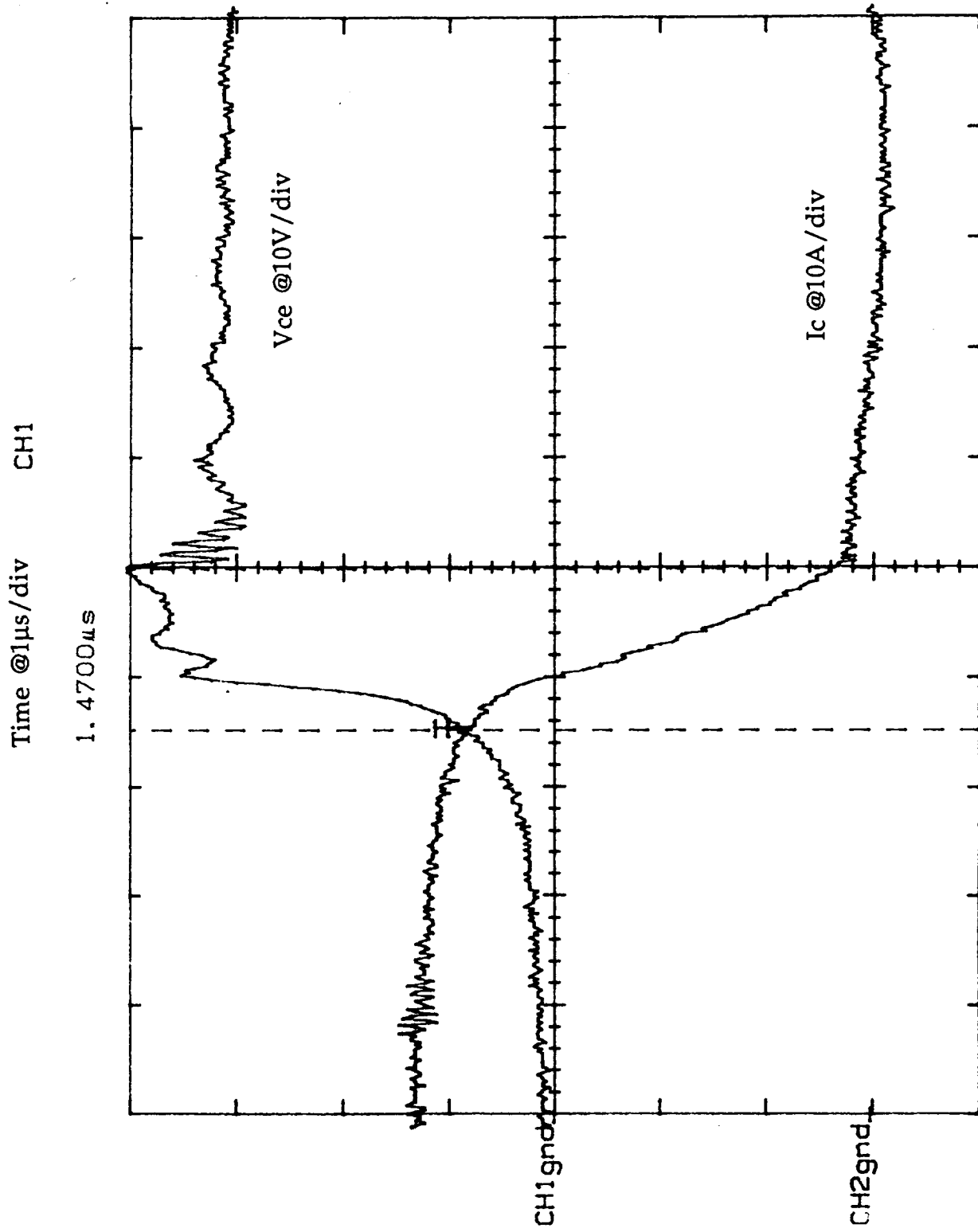
Figure 11. 2N6032 BJT turn off at 200°C (1.47μs 90-10% Ic fall-time).

Time @1μs/div   CH1

3. 1700μs

Vce @10V/div

CH1gnd

Ic @10A/div
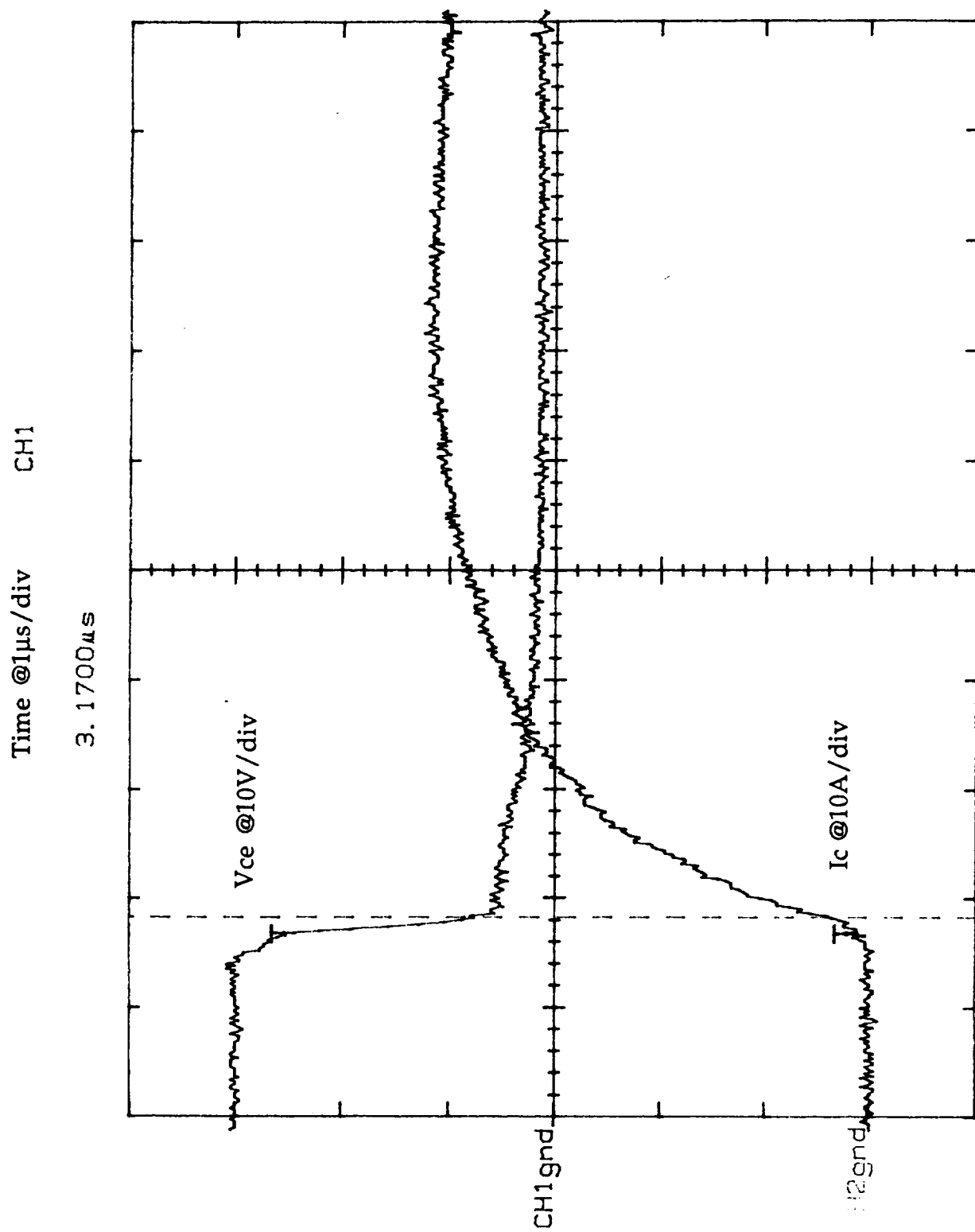
Figure 12. 2N6032 BJT turn on at 200°C (3.17μs 10-90% Ic rise-time).
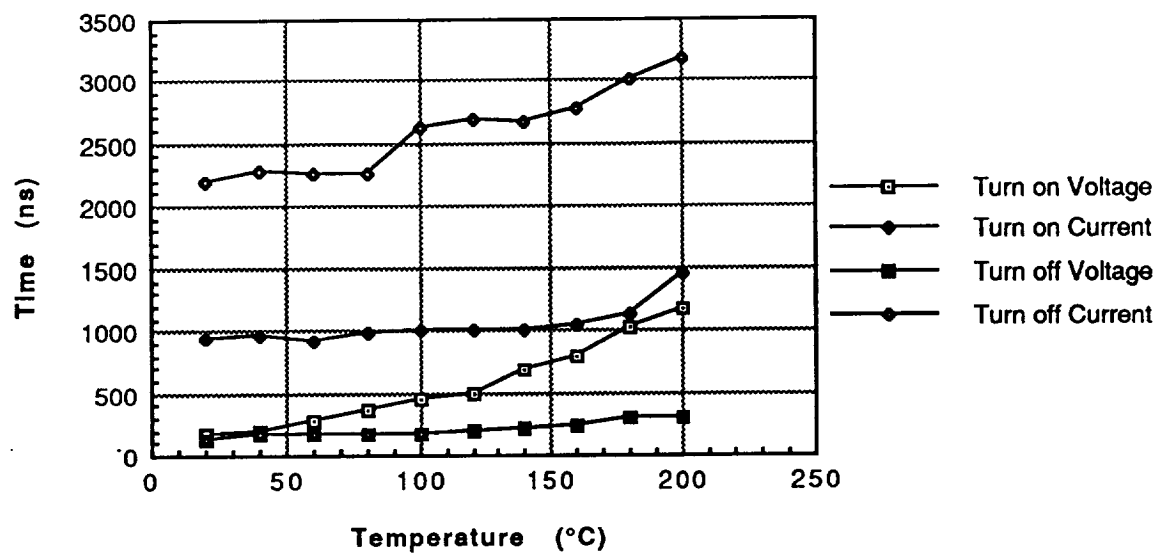
Figure 13. Resistive switching times for BJT (RL=0.67Ω L=0.212μH).

Time @200ns/div   CH1

.570.00ns

Ic @6.7A/div

Vce @30V/div

gnd
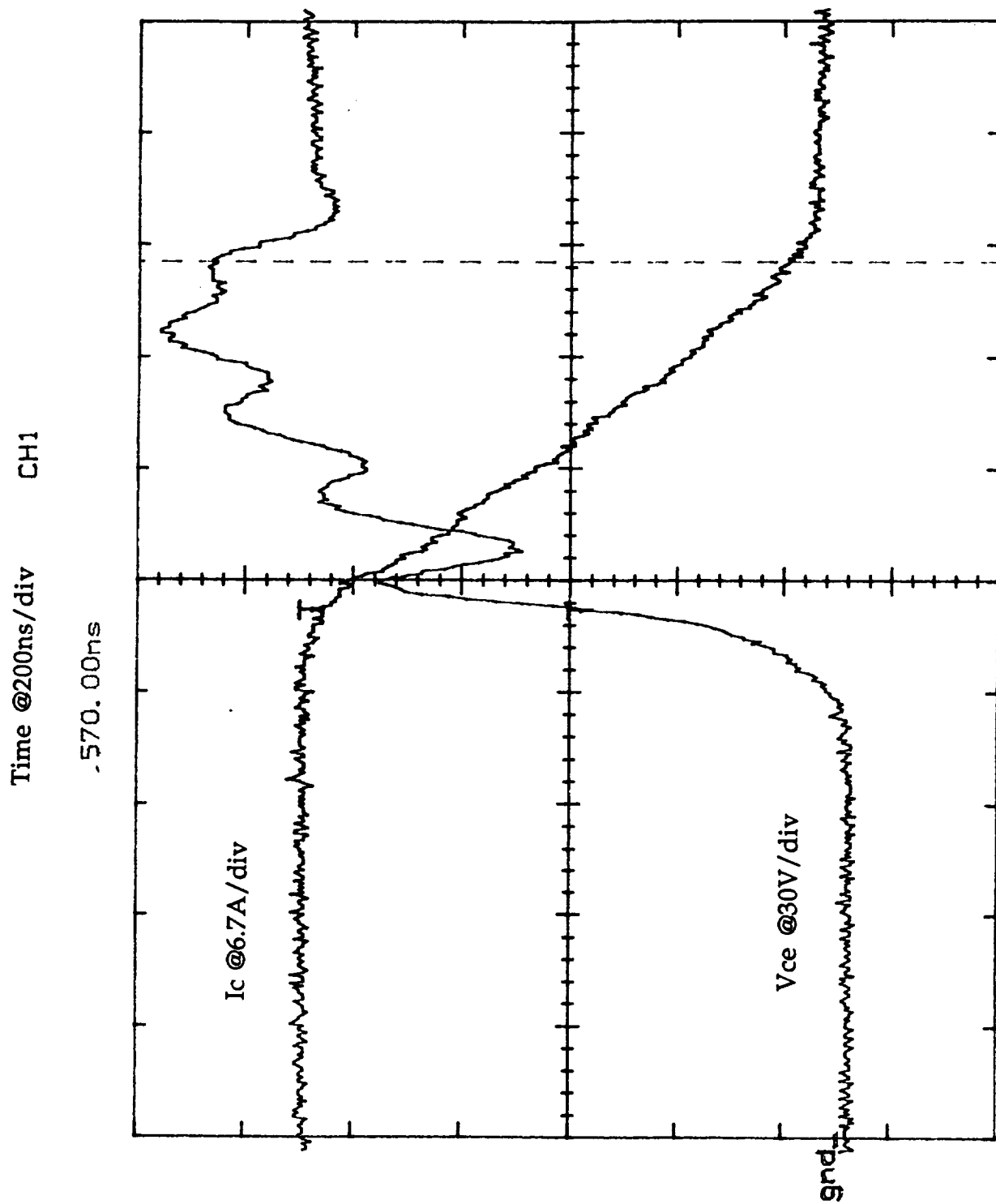
Figure 14. TA9796 IBJT turn off at 20°C (570ns 90-10% Ic fall-time).

Time @200ns/div   CH1

1.6540µs

Ic @6.7A/div

Vce @30V/div

gnd

Figure 15. TA9796 IBJT turn on at 20°C (1.654µs 10-90% Ic rise-time).

1.7420us

Vce @50V/div

CH1gnd

Ic @5A/div

CH2gnd
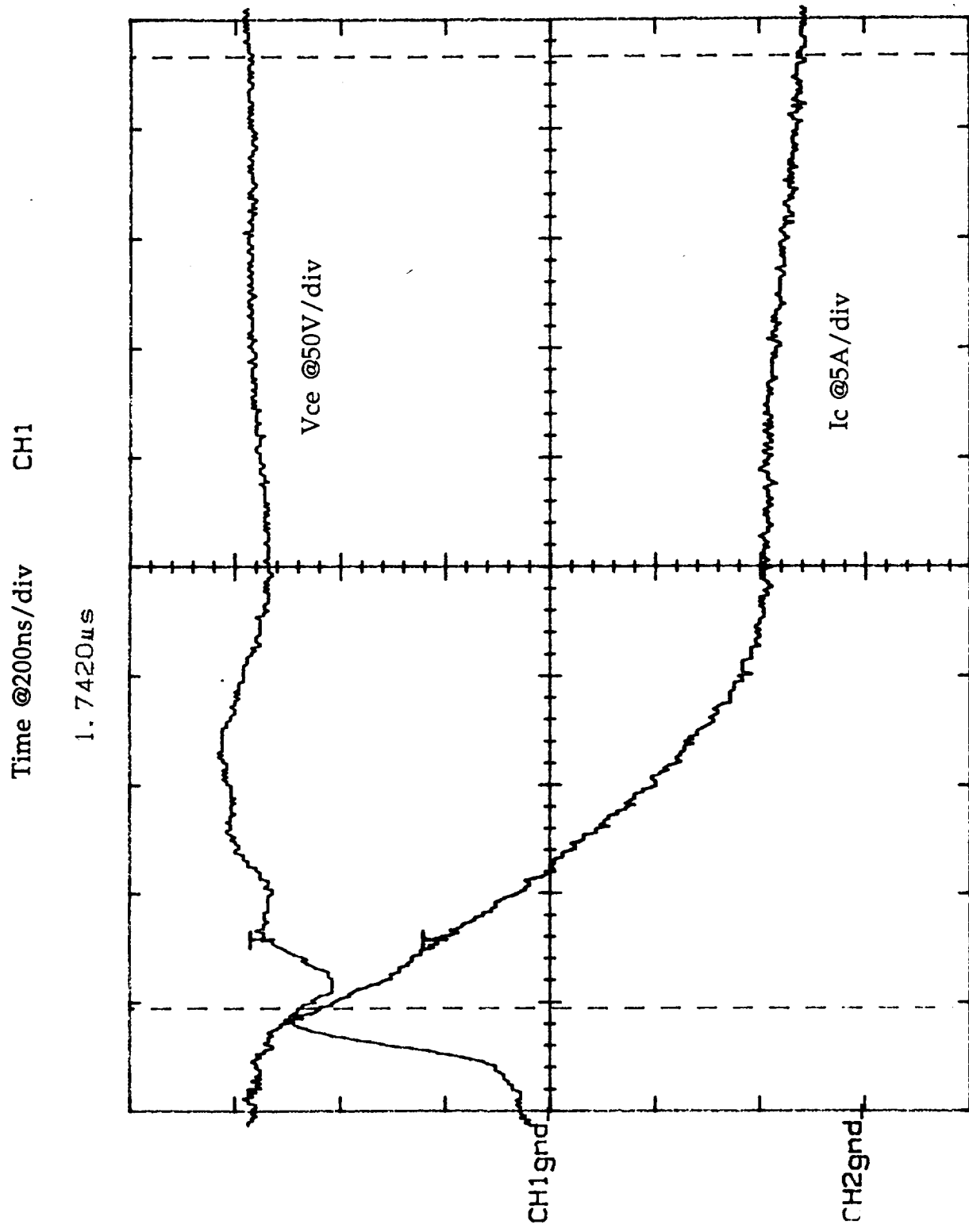
Figure 16. TA9796 IBJT turn off at 200°C (1.742µs 90-10% Ic fall-time).

Time @200ns/div   CH1

1.4280μs

Vce @50V/div

Ic @5A/div

CH1gnd

CH2gnd
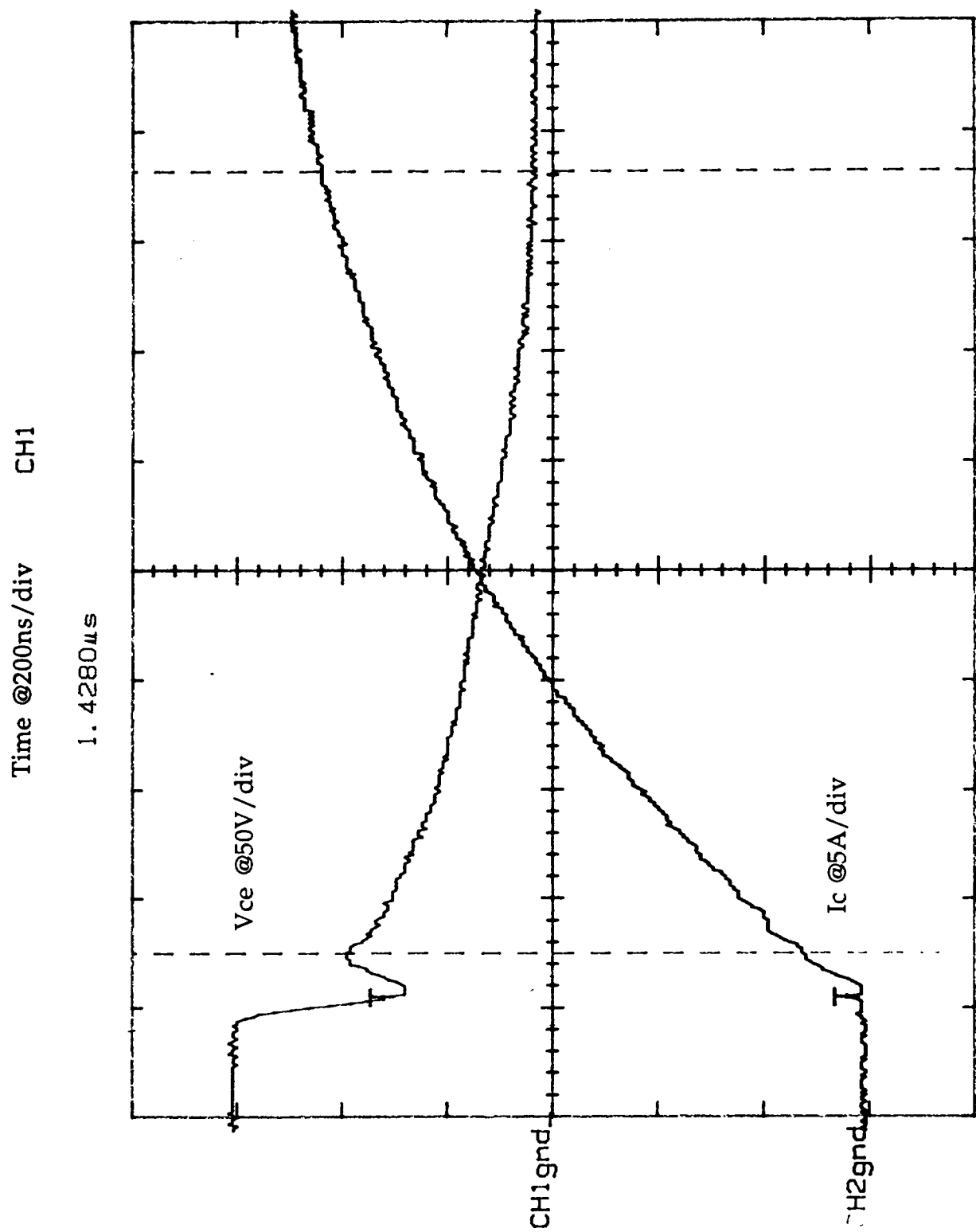
Figure 17. TA9796 IGBT turn on at 200°C (1.428μs 10-90% Ic rise-time).
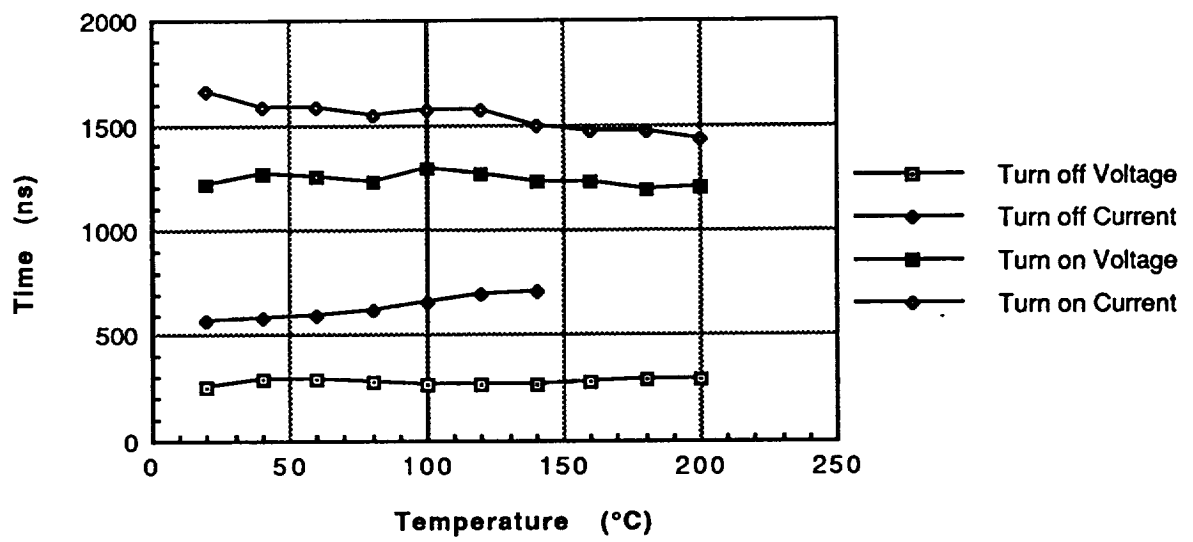
Figure 18. Resistive switching times for IGBT (RL=5.56Ω L=1.21µH).

Figure 19. H-bridge control circuitry.
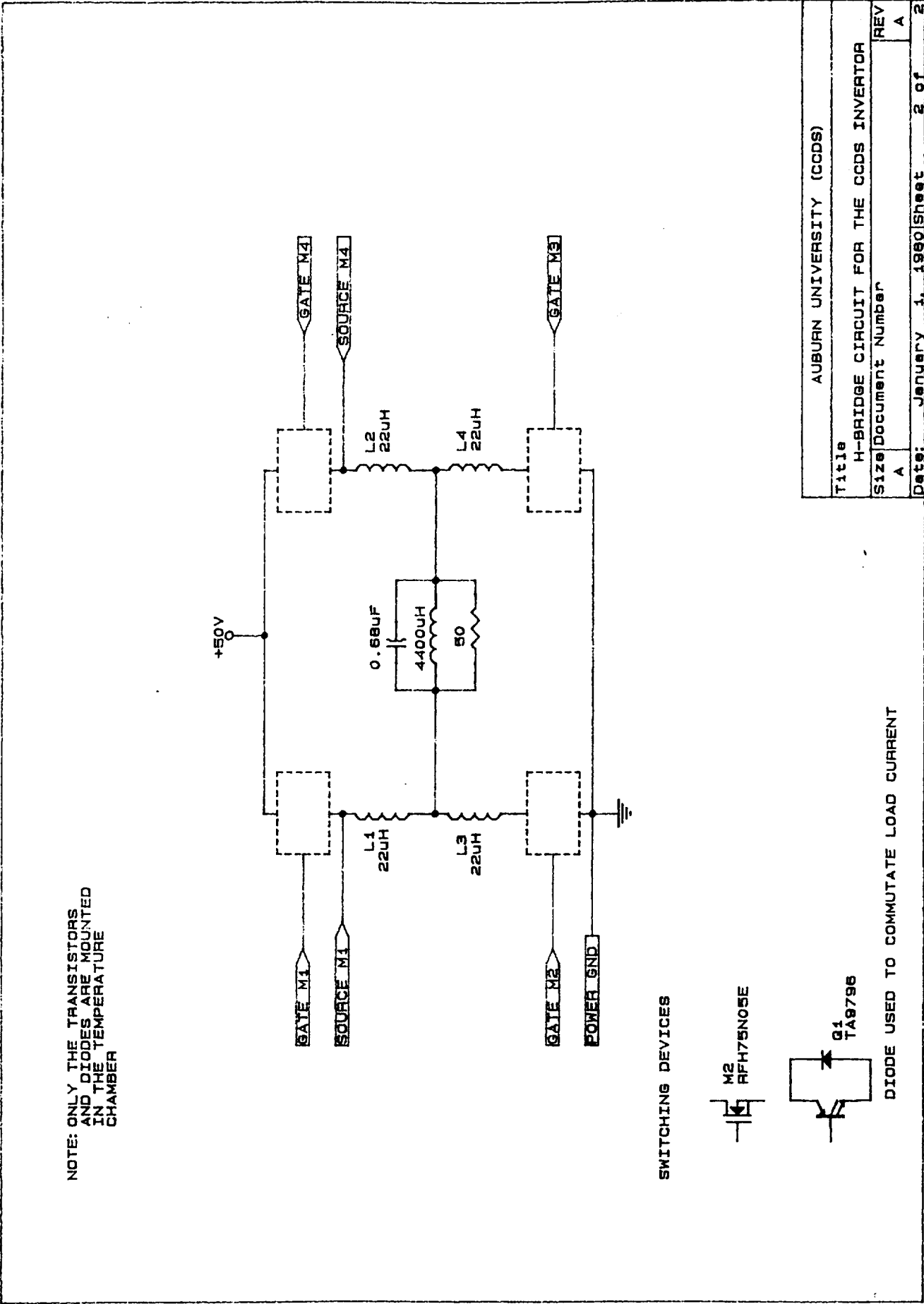
Figure 20. H-bridge schematic.

CH1   20V   A 10μs 9.06 V   CH1
CH2   10V
                                   21.552kHz
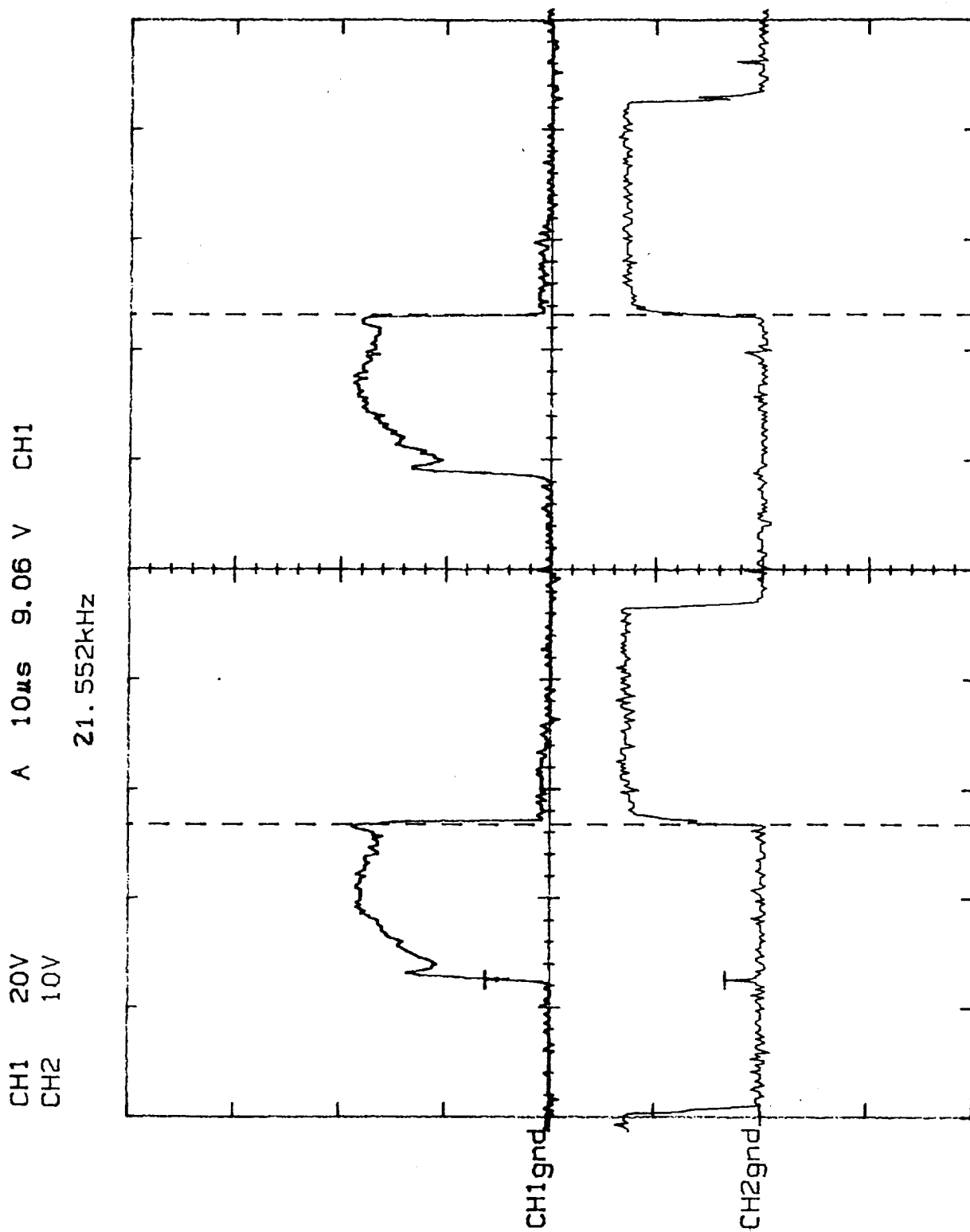
Figure 21. Vds and Vgs of low-side device, M3.

CH1   20V
CH2   10V

A   10μs   11.3 V   CH1

CH1

CH1gnd

CH2gnd
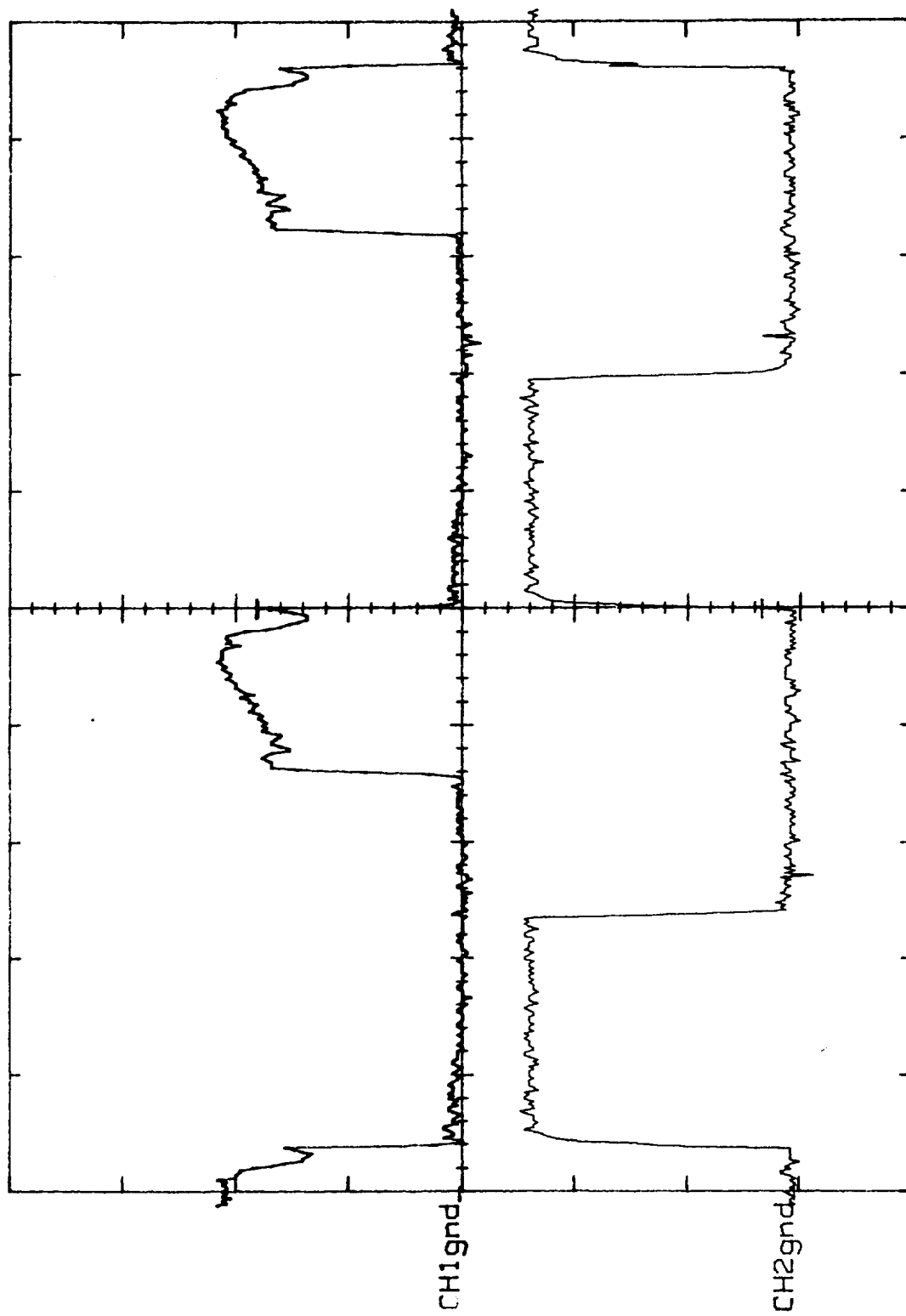
Figure 22. Vds and Vgs of high-side device, M4.

CH1   20V   A   10µs   6.25 V   CH1
CH2   10mV/Ω

Gnd

CH2gnd
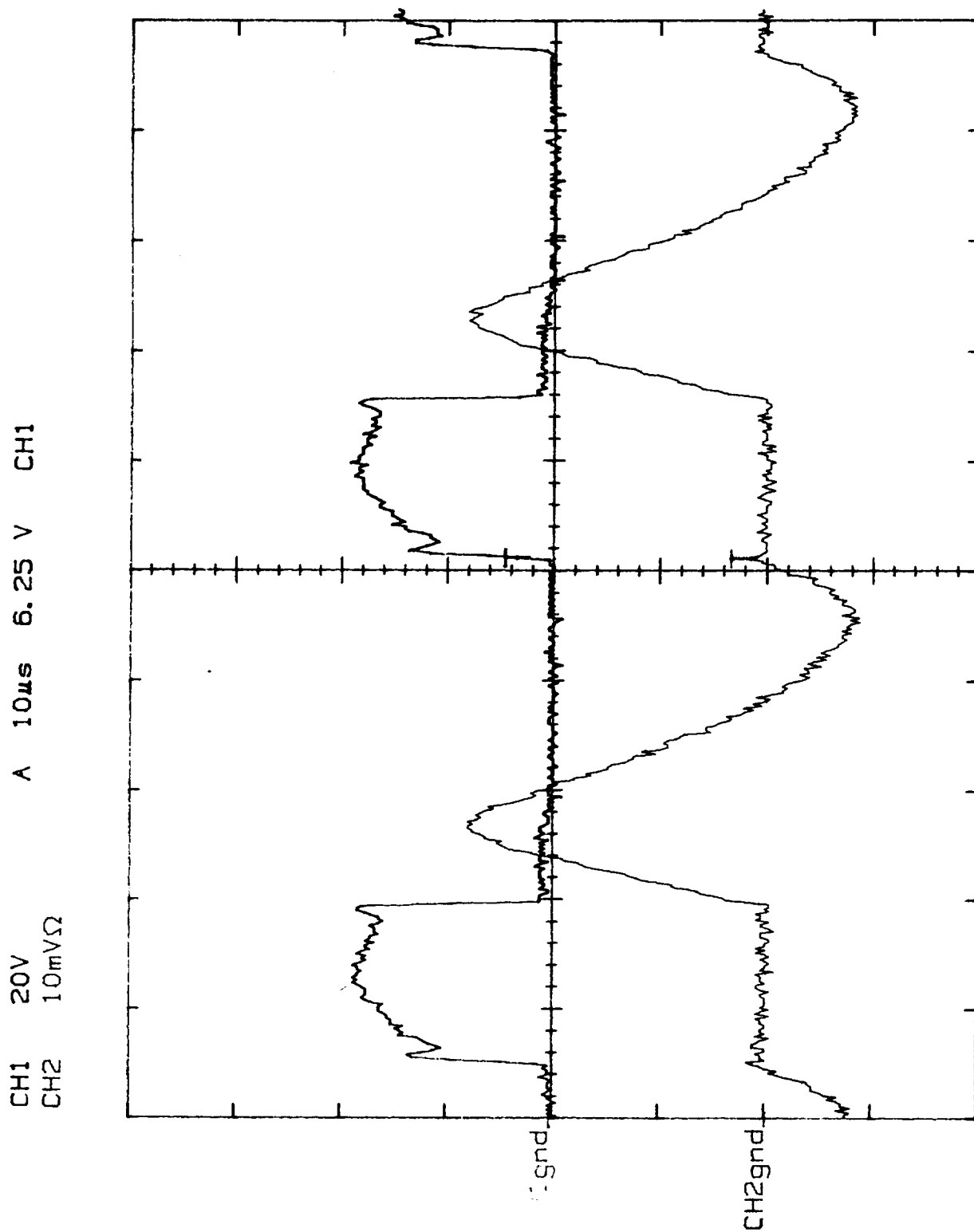
Figure 23. Vds and Id of low-side device, M3.
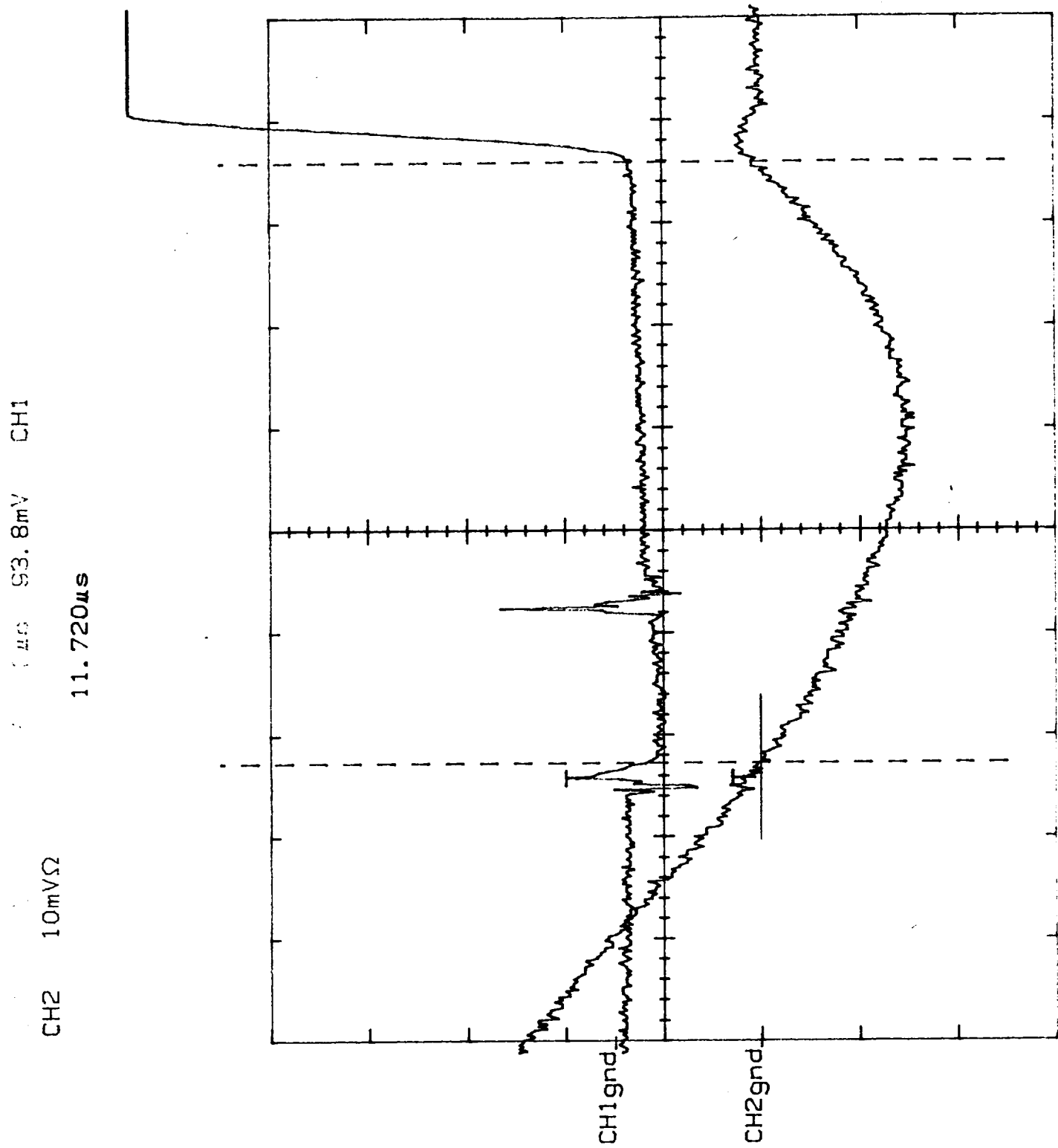
Figure 24. Forward conduction characteristic of body diode.
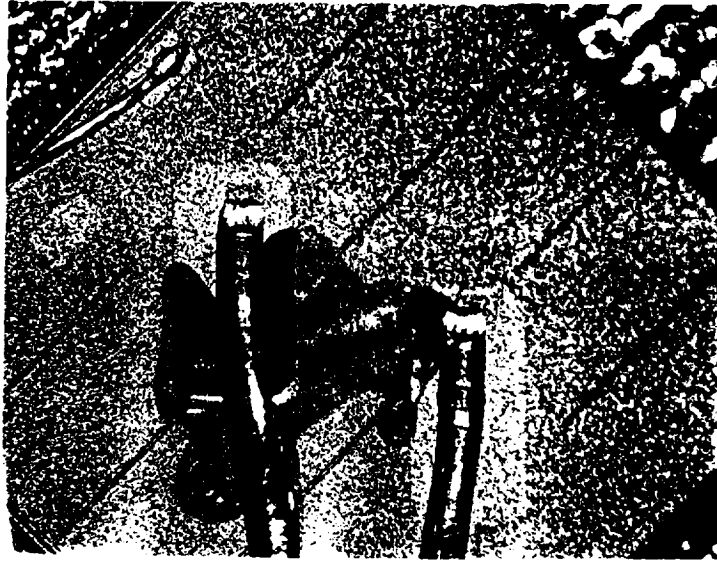
Figure 25. Optical photo of metalization failure in NMOS
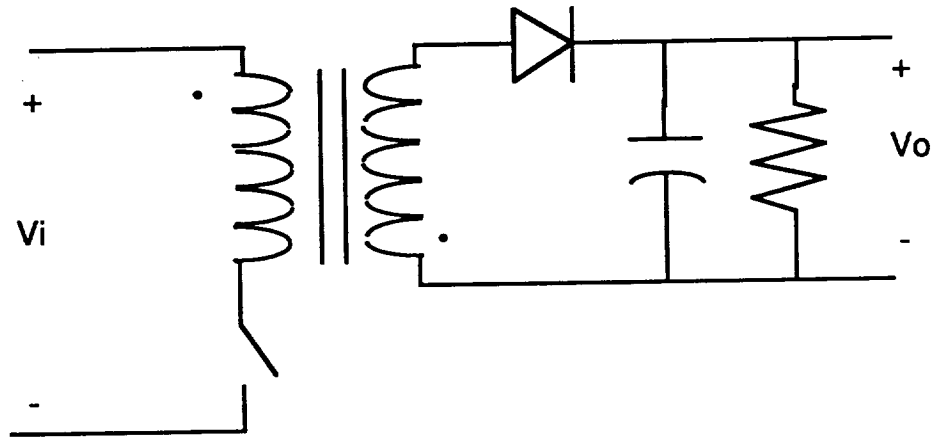
Figure 26. Flyback converter topology.

CH1   10mVΩ
CH2   20V
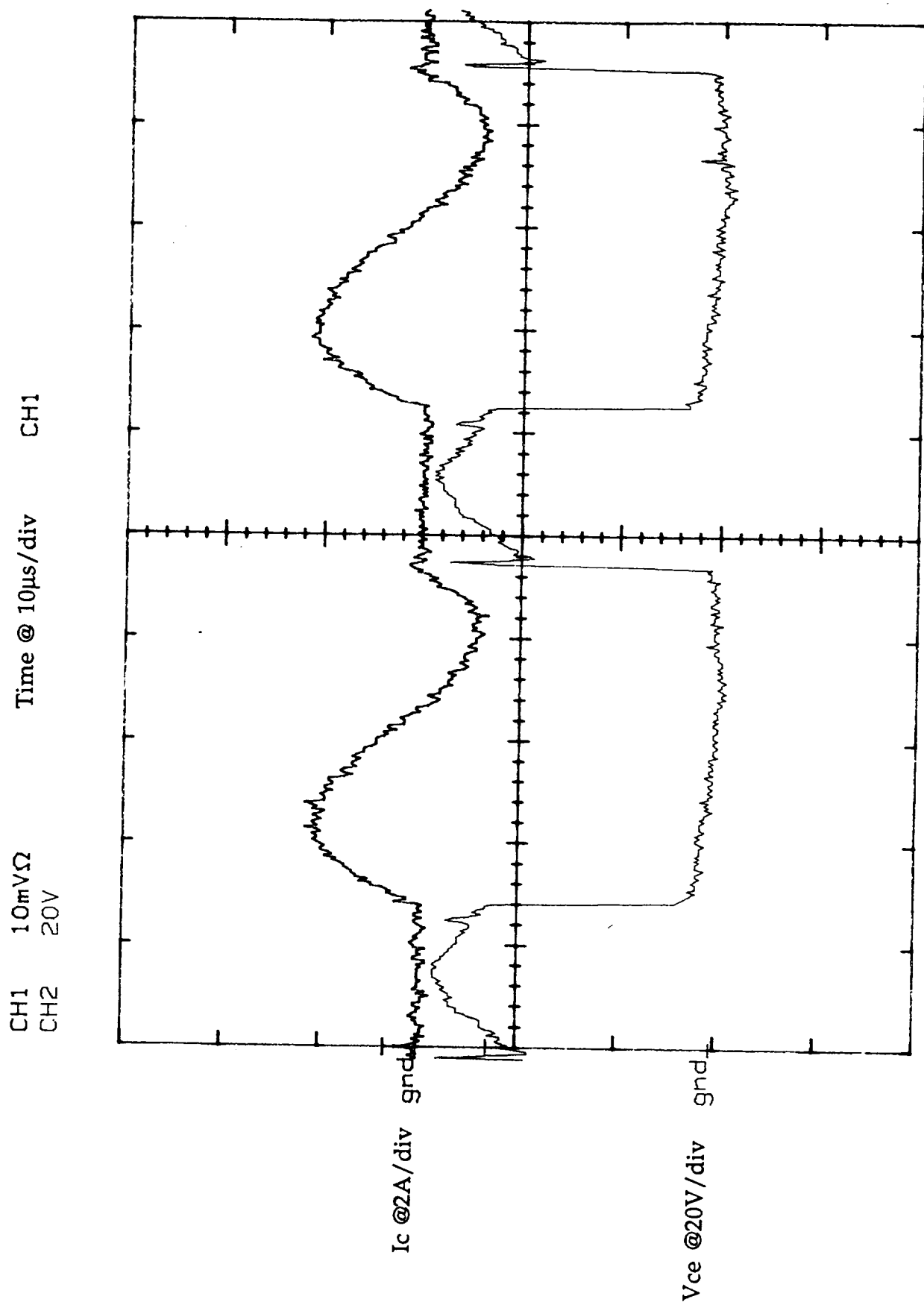
Time @ 10µs/div   CH1

Ic @2A/div

Vce @20V/div
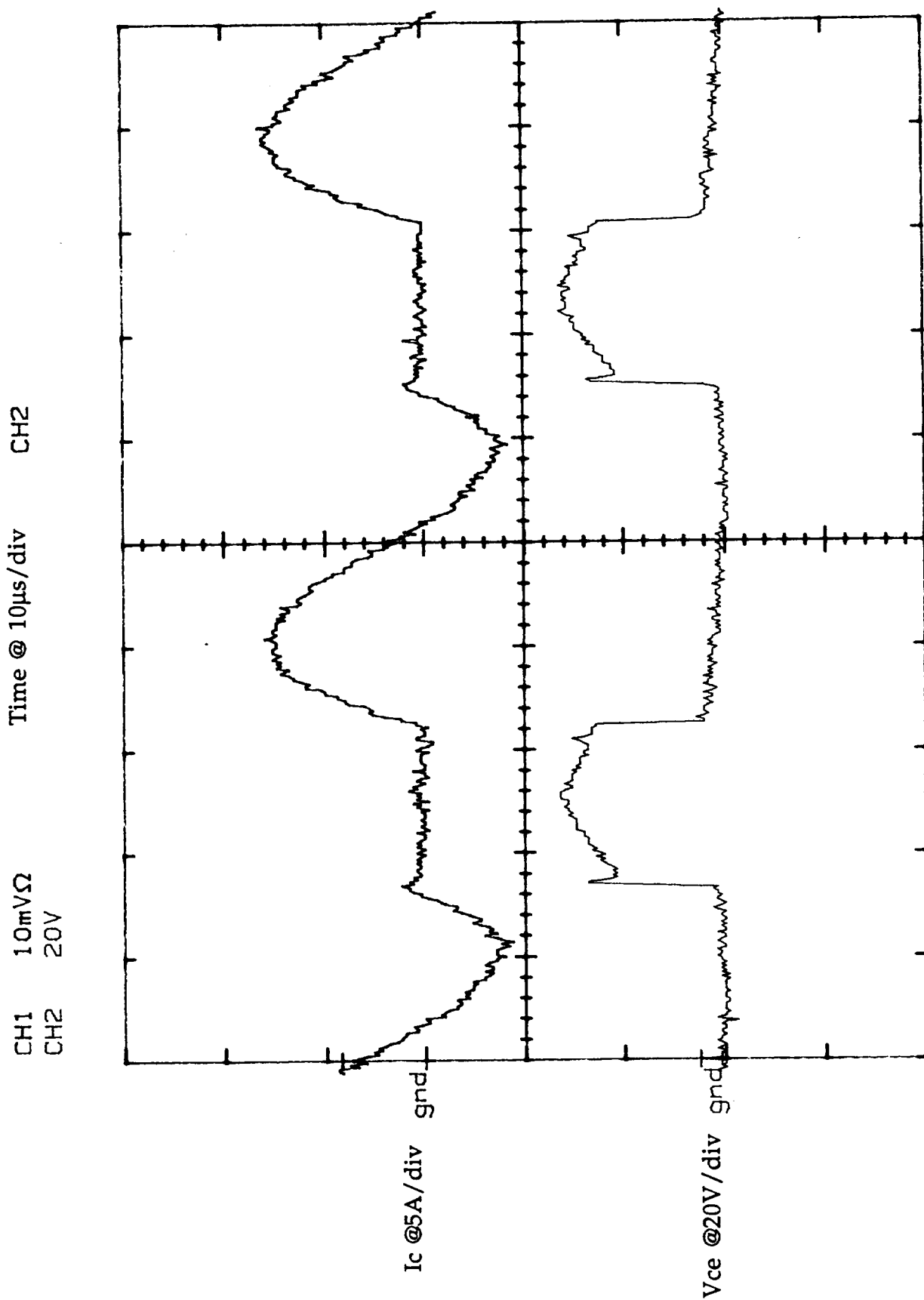
Figure 27. Id (2A/div) and Vds (20V/div) of low-side IGBT device M3 at 200°C.

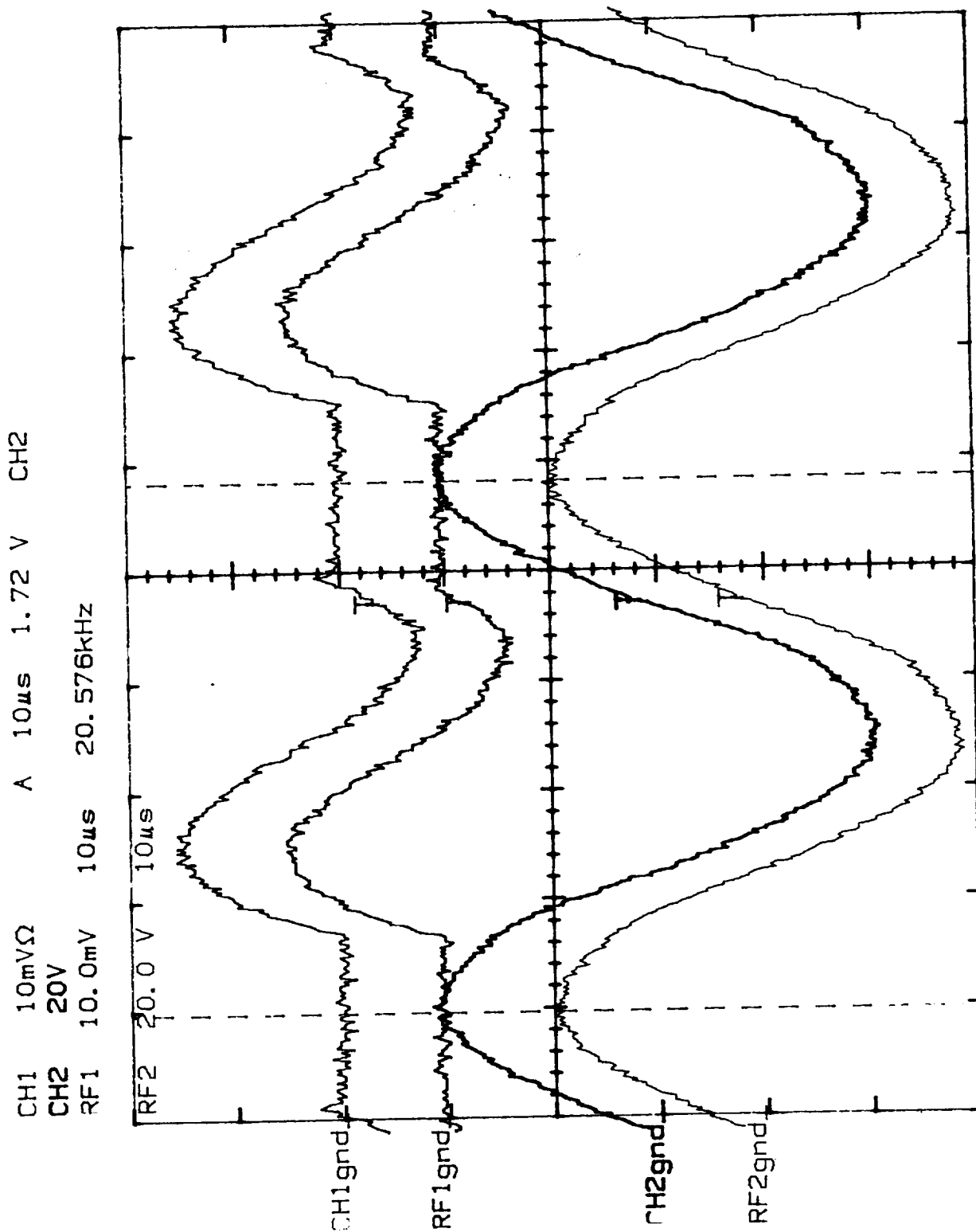Figure 28. Id (5A/div) and Vds (20V/div) of low-side IGBT device M3 at 200°C.

CH1   10mVΩ   A 10μs 1.72 V   CH2
CH2   20V
RF1   10.0mV   10μs 10μs

RF2 20.0 V   20.576kHz

CH1gnd

RF1gnd

CH2gnd

RF2gnd

Figure 29. Ic (2A/div) and Vload (20V/div) for IGBT H-Bridge at at 20 and 200°C
Top traces Ic (20°C) and Ic (200°C), Bottom traces Vload (20°C) and
Vload (200°C)